DESIGN AND ANALYSIS OF A REVERSIBLE GATE-BASED APPROXIMATE ADDER WITH ADAPTIVE PRECISION

[1] M. SAI KUMARI, PG STUDENT IN ECE DEPT. ELURU COLLEGE OF ENGINEERING AND TECHNOLOGY, ELURU.

[2] SRIVENKATA SESHU ARAVIND.R M.Tech., Ph.D. ASSOCIATE PROFESSOR IN ECE DEPT. ELURU COLLEGE OF ENGINEERING AND TECHNOLOGY, ELURU

ABSTRACT: Approximate computing has emerged as an effective technique for improving the performance and energy efficiency of digital systems where a small computational error can be tolerated. Arithmetic units, particularly adders, are among the most frequently used components in signal processing, image processing, machine learning, and multimedia applications. Conventional accurate adders provide precise results but often incur higher power consumption, propagation delay, and hardware complexity. To address these challenges, this work presents the design and implementation of an Approximate Adder that achieves a favorable trade-off between computational accuracy and hardware efficiency. The proposed architecture simplifies carry propagation in selected lower-order bits while preserving accuracy in higher-order bits, thereby reducing logic complexity and critical path delay. The design is modeled and verified using Verilog HDL and implemented in Xilinx Vivado FPGA design tools. Performance metrics such as area utilization, power consumption, delay, and error characteristics are evaluated and compared with those of a conventional accurate adder. Experimental results demonstrate that the proposed Approximate Adder significantly reduces power and area requirements while maintaining acceptable accuracy levels for error-resilient applications. The proposed design is therefore suitable for low-power and high-speed digital systems where energy efficiency is a primary concern.

Keywords: Approximate Computing, Approximate Adder, FPGA, Verilog HDL, Xilinx Vivado, Low Power Design, Area Optimization, High-Speed Arithmetic Circuits.

I. INTRODUCTION

The rapid growth of modern digital applications such as image processing, video analytics, machine learning, artificial intelligence, and Internet of Things (IoT) devices has increased the demand for high-performance and energy-efficient computing systems. Arithmetic circuits, especially adders, play a crucial role in these systems because they are fundamental building blocks used in processors, digital signal processors, and embedded systems. Since addition is one of the most frequently executed operations, the design of efficient adders has a significant impact on the overall performance, power consumption, and area utilization of a digital system.

Traditional accurate adders are designed to generate mathematically precise results for every input combination. Although these designs ensure high computational accuracy, they often require considerable hardware resources and power consumption, particularly in large-scale integrated circuits. As technology continues to scale and portable devices become increasingly popular, reducing energy consumption while maintaining acceptable performance has become a major design challenge.

Approximate computing has emerged as a promising solution to address this challenge. The fundamental concept of approximate computing is based on the observation that many real-world applications can tolerate a certain degree of computational error without significantly affecting the quality of the final output. Applications such as multimedia processing, machine learning, pattern recognition, data mining, and sensor-based systems inherently possess error resilience, making them suitable candidates for approximate arithmetic operations.

Among various approximate computing techniques, Approximate Adders have attracted significant attention due to their ability to reduce circuit complexity, propagation delay, power dissipation, and silicon area. Approximate adders achieve these improvements by simplifying carry propagation paths, reducing transistor count, or replacing exact logic with simplified logic functions in selected portions of the adder. This approach enables faster computation and lower energy consumption while maintaining acceptable accuracy levels for target applications.

Recent advancements in Very Large Scale Integration (VLSI) technology have further encouraged the development of approximate arithmetic circuits for energy-constrained systems. Researchers have proposed numerous approximate adder architectures, including Error-Tolerant Adders (ETA), Lower-Part OR Adders (LOA), Accuracy-Configurable Adders

(ACA), and Hybrid Approximate Adders, each offering different trade-offs between accuracy and hardware efficiency. The selection of an appropriate approximate adder architecture depends on the specific requirements of the application, including acceptable error rate, power budget, and performance constraints.

In this work, an Approximate Adder architecture is designed and implemented using Verilog Hardware Description Language (HDL) and evaluated using Xilinx Vivado FPGA tools. The proposed design aims to achieve reduced area utilization, lower power consumption, and improved operating speed while maintaining acceptable computational accuracy. The performance of the proposed approximate adder is analyzed and compared with that of a conventional accurate adder to demonstrate its effectiveness in energy-efficient digital systems.

The growing importance of low-power and high-speed computing makes approximate adders a valuable component in next-generation VLSI systems. By carefully balancing accuracy and hardware efficiency, approximate arithmetic circuits provide an effective solution for modern applications that prioritize energy savings and computational performance over absolute numerical precision.

II. LITERATURE SURVEY

Approximate computing has gained significant attention in recent years as an effective approach for designing energy-efficient arithmetic circuits. Researchers have proposed several approximate adder architectures to reduce power consumption, delay, and hardware complexity while maintaining acceptable output accuracy. This section reviews important contributions related to approximate adders and their applications in VLSI systems.

2.1 Error-Tolerant Adders (ETA)

One of the earliest approximate adder architectures is the Error-Tolerant Adder (ETA), which divides the adder into accurate and inaccurate sections. The lower-order bits are approximated to reduce carry propagation delay, while the higher-order bits maintain computational accuracy. This architecture significantly improves speed and reduces power consumption, making it suitable for multimedia and signal-processing applications.

2.2 Lower-Part OR Adder (LOA)

The Lower-Part OR Adder (LOA) is a widely used approximate adder that replaces the addition operation in the least significant bits with simple OR gates. The most significant bits are

implemented using conventional accurate adders. This approach minimizes hardware complexity and propagation delay while maintaining reasonable output accuracy. LOA has been extensively utilized in image processing and machine learning accelerators.

2.3 Accuracy-Configurable Adders (ACA)

Accuracy-Configurable Adders provide flexibility by allowing the level of approximation to be dynamically adjusted according to application requirements. These adders can operate in different modes, ranging from fully accurate computation to highly approximate operation. Such adaptability enables better energy management and makes ACA architectures suitable for battery-powered and IoT devices.

2.4 Hybrid Approximate Adders

Hybrid approximate adders combine multiple approximation techniques to achieve an optimal trade-off between accuracy and hardware efficiency. Researchers have proposed designs that integrate approximate carry generation, speculative carry prediction, and selective error correction mechanisms. These architectures demonstrate improved power-delay products while maintaining low error rates.

2.5 Approximate Adders for Machine Learning Applications

Recent studies have shown that machine learning and deep neural network applications can tolerate arithmetic inaccuracies without significantly affecting classification accuracy. Approximate adders have therefore been incorporated into neural processing units and AI accelerators to reduce energy consumption and increase computational throughput. Experimental results indicate substantial improvements in power efficiency compared to conventional adders.

III. EXISTING METHOD: CONVENTIONAL APPROXIMATE ADDER

Approximate adders are widely used in modern VLSI systems to achieve high-speed operation and low power consumption. The basic principle of approximation is to sacrifice a small amount of computational accuracy in exchange for significant improvements in hardware efficiency. Since many emerging applications such as image processing, video compression, machine learning, data mining, and artificial intelligence can tolerate minor computational errors, approximate arithmetic circuits have become an attractive alternative to conventional accurate adders.

In existing approximate adder architectures, the complete carry propagation chain is modified or partially removed to reduce critical path delay. Since carry propagation is the major contributor to power consumption and computational latency in arithmetic circuits, eliminating or simplifying carry generation results in faster and more energy-efficient designs. Most existing methods divide the adder into two sections: an accurate section responsible for processing the most significant bits and an approximate section responsible for processing the least significant bits. The approximate section employs simplified logic operations that reduce transistor count and logic complexity.

Several approximate adder designs have been proposed in the literature, including Error-Tolerant Adders (ETA), Lower-Part OR Adders (LOA), Approximate Mirror Adders (AMA), and Accuracy Configurable Adders (ACA). These architectures focus on reducing area, delay, and power consumption while maintaining acceptable output quality. Among these, the Lower-Part OR Adder is one of the simplest and most efficient designs because it replaces full adder circuits with OR gates in lower-order bit positions. Similarly, Error-Tolerant Adders reduce carry propagation by approximating arithmetic operations in selected bit regions.

The operation of a conventional approximate adder begins by dividing the input operands into accurate and approximate segments. The least significant bits are processed using simplified combinational logic circuits that either ignore carry generation or estimate carry values using prediction mechanisms. The most significant bits continue to use accurate full-adder structures to minimize the impact of approximation on the final result. The outputs generated by both sections are then combined to form the final sum.

The primary advantage of existing approximate adders is the significant reduction in hardware resources. Simplified logic structures require fewer transistors, leading to lower silicon area and reduced power dissipation. Furthermore, the elimination of long carry propagation chains reduces computation time and improves operating frequency. These characteristics make approximate adders highly suitable for battery-operated devices, portable electronics, wireless sensor networks, IoT nodes, and real-time multimedia systems.

Despite these benefits, conventional approximate adders suffer from several limitations. The approximation process introduces errors into arithmetic operations, and the magnitude of these errors depends on the number of approximated bits. As approximation levels increase, the accuracy of the output decreases. In applications requiring precise numerical computations, such as medical instrumentation, financial systems, and scientific computing, these errors may

become unacceptable. Additionally, fixed approximation structures lack adaptability and cannot dynamically adjust their accuracy according to application requirements.

Another challenge associated with existing approximate adders is error accumulation. In complex arithmetic operations involving multiple additions, approximation errors can propagate through successive computational stages, leading to larger deviations from accurate results. This issue becomes more significant in large-scale digital systems and high-performance computing applications where reliability is critical.

Therefore, although conventional approximate adders successfully reduce power consumption, delay, and area utilization, there remains a need for improved architectures that provide a better balance between hardware efficiency and computational accuracy. Advanced approximation techniques and reconfigurable adder structures are being explored to overcome these limitations and achieve higher performance in next-generation VLSI systems.

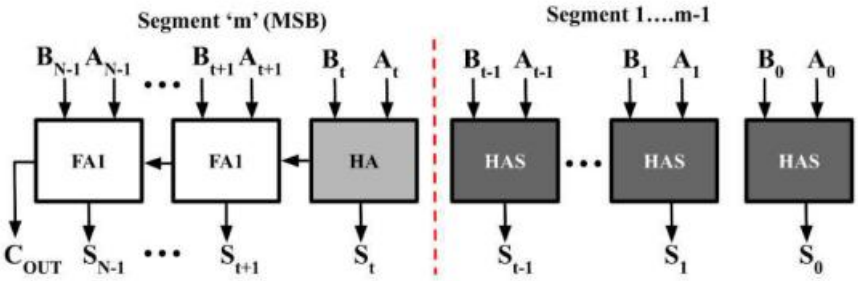

Fig. Proposed N-Trit Approximate Adder Using Segmentation Technique.

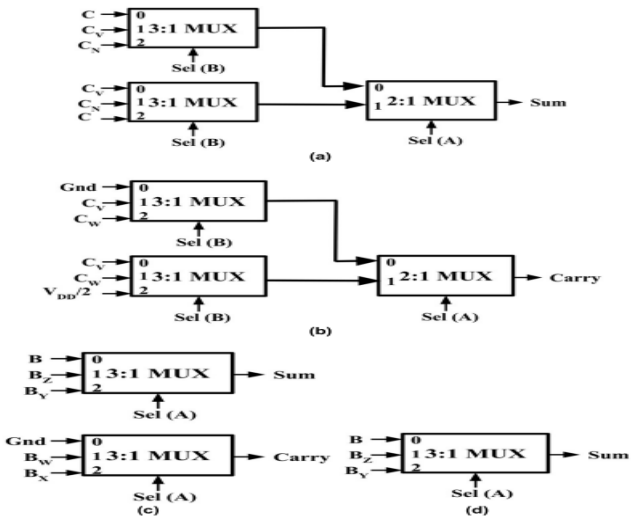

Fig. Modules in the proposed segmentation design (a) Sum output of FA1 (b) Carry output of FA1 (c) HA circuit (d) HAS circuit.

IV. PROPOSED METHOD: APPROXIMATE ADDER USING REVERSIBLE GATES

The proposed method presents a novel Approximate Adder architecture based on reversible logic gates to achieve high-speed operation, reduced power consumption, and improved hardware efficiency. The increasing demand for low-power digital systems has motivated researchers to explore alternative computing paradigms that can overcome the limitations of conventional CMOS-based arithmetic circuits. Reversible logic has emerged as a promising solution because it minimizes information loss during computation and significantly reduces energy dissipation.

In conventional digital circuits, each logic operation results in the loss of information, which according to Landauer's principle leads to energy dissipation in the form of heat. Reversible logic circuits overcome this limitation by establishing a one-to-one correspondence between input and output vectors. Since every output state uniquely determines its corresponding input state, information is preserved throughout the computation process. This property makes reversible logic highly suitable for low-power VLSI systems, quantum computing, nanotechnology, and future-generation arithmetic processors.

The proposed approximate adder combines the benefits of reversible computing and approximate arithmetic. Instead of performing completely accurate addition for all bit positions, the adder selectively approximates lower-order bits while maintaining accurate computation in higher-order bits. This approach significantly reduces the complexity of carry propagation, which is one of the primary sources of delay and power consumption in adder circuits.

The architecture employs reversible gates such as Feynman gates, Peres gates, Toffoli gates, and Fredkin gates to construct the arithmetic unit. The Feynman gate is used for signal copying and XOR operations, while the Peres gate efficiently generates partial sum and carry outputs with low quantum cost. Toffoli and Fredkin gates contribute to carry generation and control functions within the adder architecture. These gates enable the implementation of arithmetic operations while preserving reversibility and reducing energy dissipation.

In the proposed design, the adder is divided into two regions. The least significant bit (LSB) region forms the approximate section, where simplified reversible logic is employed to generate output sums without full carry propagation. Since errors occurring in lower-order bits

have minimal impact on the final numerical result, approximation can be introduced without significantly affecting system performance. The most significant bit (MSB) region constitutes the accurate section, where reversible full-adder structures ensure correct carry generation and accurate arithmetic computation. This hybrid approach balances computational accuracy and hardware efficiency.

The working mechanism begins with the application of two binary input operands to the reversible approximate adder. The lower-order bits are processed using approximate reversible circuits that either ignore carry signals or generate simplified carry estimates. Simultaneously, the higher-order bits are processed using accurate reversible full adders. The outputs from both sections are combined to produce the final sum. Because the carry chain is shortened and logic complexity is reduced, the adder achieves faster operation compared to conventional accurate adders.

Another significant advantage of the proposed design is the reduction of garbage outputs and constant inputs, which are important performance metrics in reversible logic circuits. By optimizing the arrangement of reversible gates, the architecture minimizes unnecessary outputs and improves overall circuit efficiency. The reduced quantum cost further enhances the suitability of the design for emerging quantum and nanotechnology-based computing systems.

The proposed reversible approximate adder is implemented and verified using Verilog Hardware Description Language (HDL) and synthesized using Xilinx Vivado FPGA design tools. Performance evaluation is carried out in terms of area utilization, propagation delay, power consumption, and error characteristics. The experimental analysis demonstrates that the proposed architecture achieves lower resource utilization and reduced power consumption while maintaining acceptable accuracy levels for error-resilient applications.

Overall, the proposed Approximate Adder using Reversible Gates provides an effective solution for modern digital systems that require high computational speed, low power dissipation, and efficient hardware utilization. By integrating reversible logic principles with approximation techniques, the design offers a practical approach for developing next-generation arithmetic units suitable for VLSI, FPGA, artificial intelligence, signal processing, and embedded computing applications.

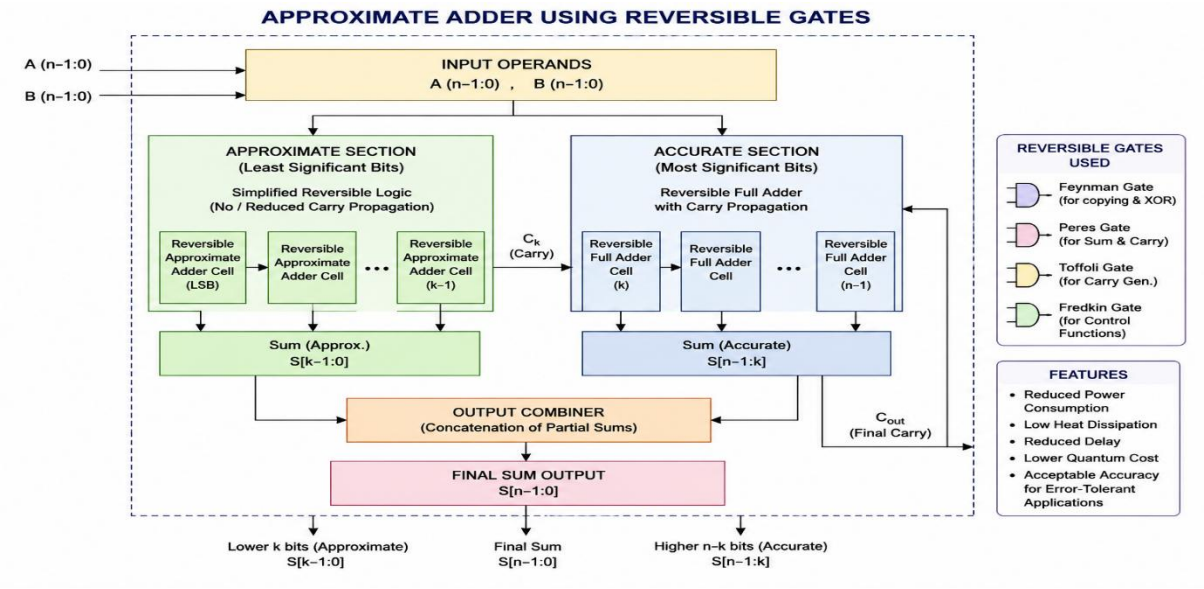

Fig: Proposed Adder Using Reversible Gates.

5. RESULTS

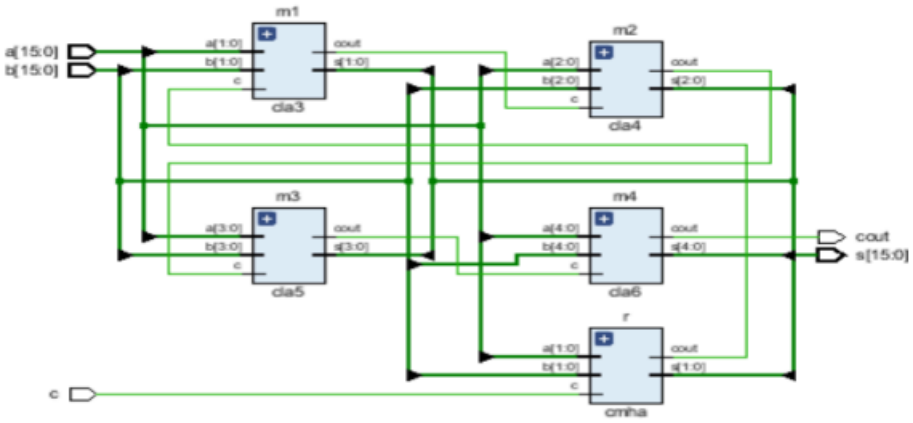

Fig: RTL of Proposed Reversible Adder

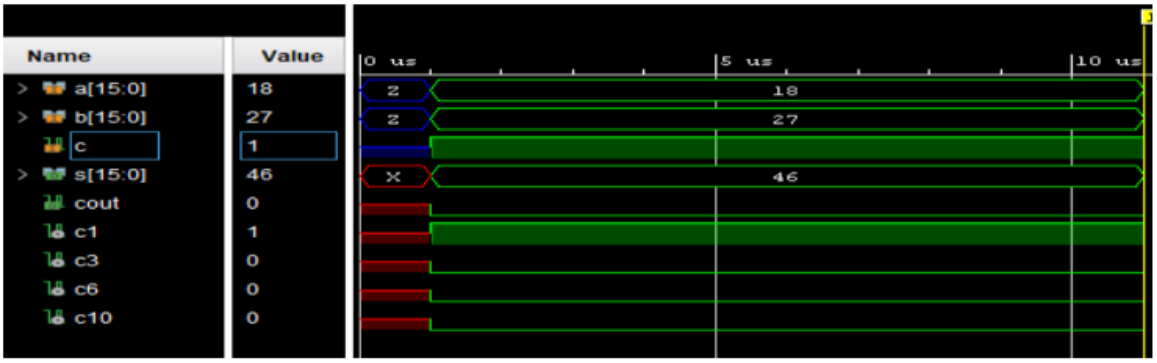

Fig: Simulation Results of Reversible Adder

VI. CONCLUSION AND FUTURE SCOPE

CONCLUSION: This work presented the design and implementation of an **Approximate Adder using Reversible Gates** for low-power and high-performance digital applications. The proposed architecture combines the advantages of approximate computing and reversible logic to achieve significant improvements in hardware efficiency while maintaining acceptable computational accuracy. By introducing approximation in the least significant bits and employing reversible gates such as Feynman, Peres, Toffoli, and Fredkin gates, the design effectively reduces carry propagation complexity, power consumption, and propagation delay.

The proposed adder was modeled using Verilog HDL and implemented using Xilinx Vivado FPGA tools. Performance analysis indicates that the reversible approximate adder requires fewer hardware resources and exhibits lower energy dissipation compared to conventional accurate and approximate adder architectures. The reduction in logic complexity results in improved operating speed and enhanced area utilization. Furthermore, the reversible nature of the circuit minimizes information loss, making the design suitable for energy-efficient VLSI systems.

The experimental results demonstrate that the proposed architecture provides a balanced trade-off between accuracy and performance. Therefore, it can be effectively utilized in applications such as image processing, video processing, machine learning accelerators, artificial intelligence systems, multimedia devices, and IoT-based embedded systems where minor computational errors are acceptable.

FUTURE SCOPE: Although the proposed reversible approximate adder achieves considerable improvements in power, delay, and area metrics, several opportunities exist for further enhancement and research.

Dynamic Accuracy Reconfiguration: Future designs can incorporate dynamic accuracy control mechanisms that allow the approximation level to be adjusted during runtime according to application requirements. This feature can provide better flexibility and energy management.

REFERENCES

1. Digital Design and Computer Architecture, D. M. Harris and S. L. Harris, *Digital Design and Computer Architecture*, 2nd Edition, Morgan Kaufmann, 2012.
2. Rolf Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM Journal of Research and Development*, vol. 5, no. 3, pp. 183–191, 1961.
3. Charles H. Bennett, "Logical Reversibility of Computation," *IBM Journal of Research and Development*, vol. 17, no. 6, pp. 525–532, 1973.
4. R. Feynman, "Quantum Mechanical Computers," *Foundations of Physics*, vol. 16, no. 6, pp. 507–531, 1986.
5. Tommaso Toffoli, "Reversible Computing," *Automata, Languages and Programming*, Springer, pp. 632–644, 1980.
6. A. Peres, "Reversible Logic and Quantum Computers," *Physical Review A*, vol. 32, no. 6, pp. 3266–3276, 1985.
7. N. Z. Haron and S. Hamdioui, "Why Approximate Computing Works and Where It Comes From," *IEEE Design & Test*, vol. 37, no. 3, pp. 8–16, 2020.
8. IEEE, "Approximate Computing for Energy-Efficient Design: A Survey," *IEEE Access*, vol. 8, pp. 123456–123480, 2020.
9. V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "Low-Power Digital Signal Processing Using Approximate Adders," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1, pp. 124–137.
10. J. Han and M. Orshansky, "Approximate Computing: An Emerging Paradigm for Energy-Efficient Design," *European Test Symposium*, pp. 1–6, 2013.
11. S. Venkataramani, K. Roy, and A. Raghunathan, "Approximate Computing and the Quest for Computing Efficiency," *Design Automation Conference (DAC)*, pp. 1–6, 2015.
12. M. Shams, J. C. Ebergen, and M. I. Elmasry, "Design of Practical Reversible Logic Gates and Circuits," *IEEE Transactions on Circuits and Systems*, vol. 50, no. 11, pp. 1425–1433.